# $I^2C$-bus controlled PAL/NTSC TV processor

# TDA8366

## FEATURES

- Multistandard vision IF circuit (positive and negative modulation)
- Video identification circuit in the IF circuit which is independent of the synchronization for stable On Screen Display (OSD) under 'no-signal' conditions
- Source selection with 2 Colour Video Blanking Synchronization (CVBS) inputs and a Y/C (or extra CVBS) input
- Output signals of the video switch circuit for the teletext decoder and a Picture-In-Picture (PIP) processor
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- Asymmetrical peaking in the luminance channel with a (defeatable) noise coring function
- PAL/NTSC colour decoder with automatic search system
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications
- RGB control circuit with black-current stabilization and white point adjustment; to obtain a good grey scale tracking the black-current ratio of the 3 guns depends on the white point adjustment
- Linear RGB inputs and fast blanking
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Geometry correction by means of modulation of the vertical and EW drive
- $I^2C$-bus control of various functions
- Low dissipation (850 mW)
- Small amount of peripheral components compared with competition ICs
- Only one adjustment (vision IF demodulator)
- Y, U and V inputs and outputs.

## GENERAL DESCRIPTION

The TDA8366 is an $I^2C$-bus controlled PAL/NTSC TV processor. The circuit has been designed for use with the baseband chrominance delay line TDA4665 and for DC-coupled vertical and East-West (EW) output stages.

The device can process both CVBS and Y/C input signals and has a linear RGB-input with fast blanking.

The peaking circuit generates asymmetrical overshoots (the amplitude of the 'black' overshoots is approximately 2 times higher as the one of the 'white' overshoots) and contains a (defeatable) coring function.

The RGB control circuit contains a black-current stabilizer circuit with internal clamp capacitors. The white point of the picture tube is adjusted via the $I^2C$-bus.

The deflection control circuit provides a drive pulse for the horizontal output stage, a differential sawtooth current for the vertical output stage and an East-West drive current for the East-West output stage.These signals can be manipulated for geometry correction of the picture.

The supply voltage for the IC is 8 V. The IC is available in an SDIP package with 52 pins and in a QFP package with 64 pins (see Chapter "Ordering information").

The pin numbers indicated in this document are referenced to the SDIP52; SOT247-1 package; unless otherwise indicated.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA8366 | SDIP52 | plastic shrink dual in-line package; 52 leads (600 mil) | SOT247-1 |
| TDA8366H | QFP64[(1)] | plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm | SOT319-2 |

**Note**

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| $V_P$ | supply voltage | – | 8.0 | – | V |
| $I_P$ | supply current | – | 100 | – | mA |
| **Input voltages** | | | | | |
| $V_{46,47(rms)}$ | video IF amplifier sensitivity (RMS value) | – | 70 | – | µV |
| $V_{15(p-p)}$ | external CVBS input (peak-to-peak value) | – | 1.0 | – | V |
| $V_{9(p-p)}$ | S-VHS luminance input voltage (peak-to-peak value) | – | 1.0 | – | V |
| $V_{8(p-p)}$ | S-VHS chroma input voltage (burst amplitude) (peak-to-peak value) | – | 0.3 | – | V |
| $V_{21,22,23(p-p)}$ | RGB inputs (peak-to-peak value) | – | 0.7 | – | V |
| **Output signals** | | | | | |
| $V_{o(p-p)}$ | demodulated CVBS output (peak-to-peak value) | – | 2.5 | – | V |
| $I_{52}$ | tuner AGC output current range | 0 | – | 5 | mA |
| $V_{36(p-p)}$ | TXT output voltage (peak-to-peak value) | – | 1.0 | – | V |
| $V_{13(p-p)}$ | PIP output voltage (peak-to-peak value) | – | 1.0 | – | V |
| $V_{28(p-p)}$ | –(R–Y) output voltage (peak-to-peak value) | – | 525 | – | mV |
| $V_{27(p-p)}$ | –(B–Y) output voltage (peak-to-peak value) | – | 675 | – | mV |
| $V_{26}$ | Y output voltage | – | 450 | – | mV |
| $V_{19,18,17(p-p)}$ | RGB output signal amplitudes (peak-to-peak value) | – | 2.0 | – | V |
| $I_{38}$ | horizontal output current | 10 | – | – | mA |
| $I_{44,45}$ | vertical output current | 1 | – | – | mA |
| $I_{43}$ | EW drive output current | 0.5 | – | – | mA |

## BLOCK DIAGRAM

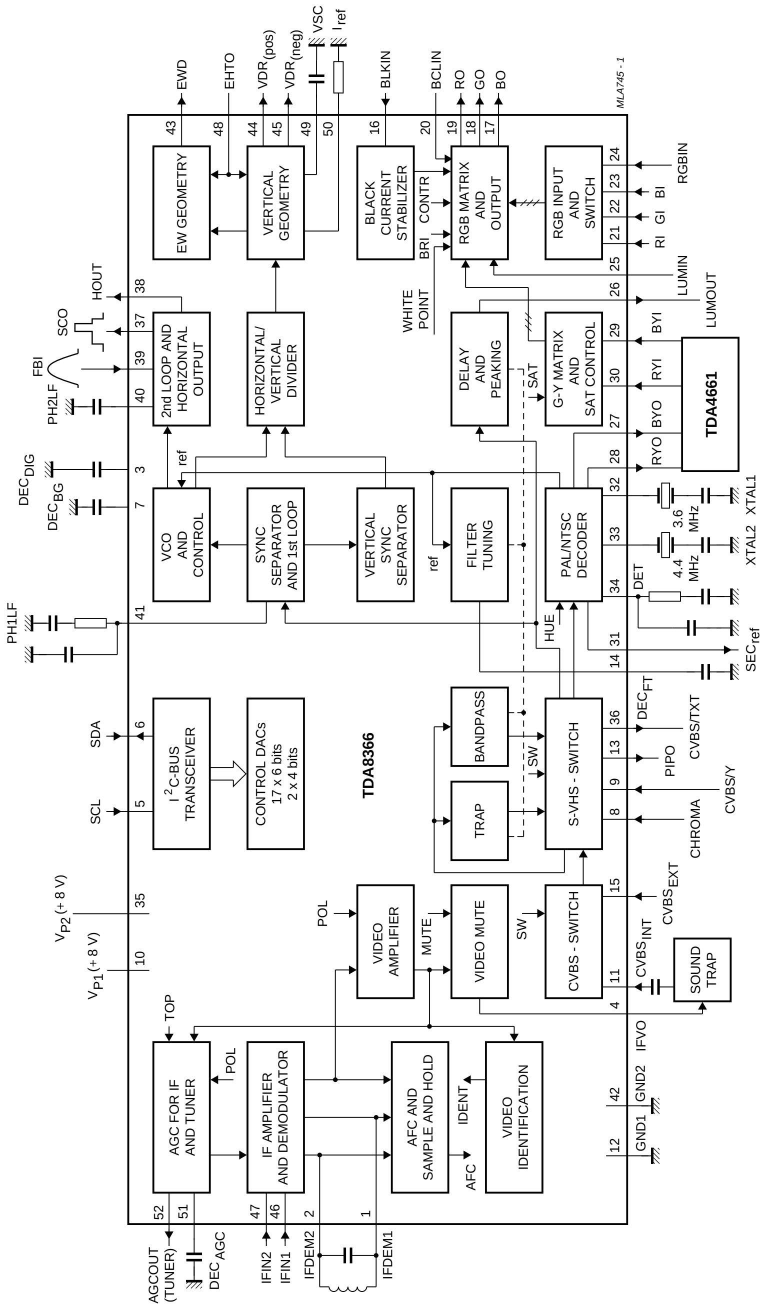



Fig.1 Block diagram (SDIP52; SOT247-1).

## PINNING

| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | SDIP52 | QFP64 | |
| IFDEM1 | 1 | 11 | IF demodulator tuned circuit 1 |
| IFDEM2 | 2 | 12 | IF demodulator tuned circuit 2 |
| $DEC_{DIG}$ | 3 | 13 | decoupling digital supply |
| IFVO | 4 | 14 | IF video output |
| SCL | 5 | 16 | serial clock input |
| SDA | 6 | 17 | serial data input/output |
| $DEC_{BG}$ | 7 | 18 | bandgap decoupling |
| CHROMA | 8 | 20 | chrominance input (S-VHS) |
| CVBS/Y | 9 | 21 | external CVBS/Y input |
| $V_{P1}$ | 10 | 22 | main supply voltage 1 (+8 V) |
| $CVBS_{INT}$ | 11 | 29 | internal CVBS input |
| GND1 | 12 | 25 | ground 1 |
| PIPO | 13 | 27 | picture-in-picture output |
| $DEC_{FT}$ | 14 | 28 | decoupling filter tuning |
| $CVBS_{EXT}$ | 15 | 24 | external CVBS input |
| BLKIN | 16 | 30 | black-current input |
| BO | 17 | 31 | blue output |
| GO | 18 | 32 | green output |
| RO | 19 | 33 | red output |
| BCLIN | 20 | 35 | beam current limiter input |
| RI | 21 | 37 | red input for insertion |
| GI | 22 | 38 | green input for insertion |
| BI | 23 | 39 | blue input for insertion |
| RGBIN | 24 | 40 | RGB insertion input |
| LUMIN | 25 | 42 | luminance input |
| LUMOUT | 26 | 43 | luminance output |
| BYO | 27 | 44 | (B–Y) signal output |
| RYO | 28 | 45 | (R–Y) signal output |
| BYI | 29 | 46 | (B–Y) signal input |
| RYI | 30 | 47 | (R–Y) signal input |
| $SEC_{ref}$ | 31 | 48 | SECAM reference output |
| XTAL1 | 32 | 49 | 3.58 MHz crystal connection |
| XTAL2 | 33 | 50 | 4.43/3.58 MHz crystal connection |
| DET | 34 | 52 | loop filter phase detector |
| $V_{P2}$ | 35 | 54 | horizontal oscillator supply voltage (+8 V) |
| CVBS/TXT | 36 | 55 | CVBS/TXT output |
| SCO | 37 | 56 | sandcastle output |
| HOUT | 38 | 57 | horizontal output |

| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | SDIP52 | QFP64 | |
| FBI | 39 | 58 | flyback input |
| PH2LF | 40 | 59 | phase-2 filter |
| PH1LF | 41 | 60 | phase-1 filter |
| GND2 | 42 | 26 | ground 2 |
| EWD | 43 | 63 | east-west drive output |
| $VDR_{(pos)}$ | 44 | 64 | vertical drive 1 positive output |
| $VDR_{(neg)}$ | 45 | 1 | vertical drive 2 negative output |
| IFIN1 | 46 | 2 | IF input 1 |
| IFIN2 | 47 | 3 | IF input 2 |
| EHTO | 48 | 4 | EHT/overvoltage protection input |
| VSC | 49 | 5 | vertical sawtooth capacitor |
| $I_{ref}$ | 50 | 6 | reference current input |
| $DEC_{AGC}$ | 51 | 7 | AGC decoupling capacitor |
| AGCOUT | 52 | 8 | tuner AGC output |
| n.c. | – | 9 | not connected |
| n.c. | – | 10 | not connected |
| n.c. | – | 15 | not connected |
| n.c. | – | 19 | not connected |
| n.c. | – | 34 | not connected |
| n.c. | – | 36 | not connected |
| n.c. | – | 41 | not connected |
| n.c. | – | 51 | not connected |
| n.c. | – | 53 | not connected |
| $V_{P3}$ | – | 23 | supply voltage 3 (+8 V) |
| GND3 | – | 61 | ground 3 |
| GND4 | – | 62 | ground 4 |

The pin numbers mentioned in the rest of this document are referenced to the SDIP52 (SOT247-1) package.

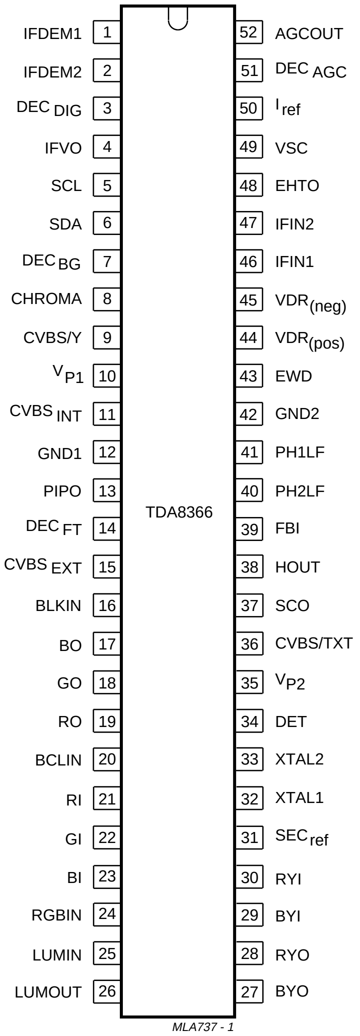



Fig.2 Pin configuration (SDIP52).

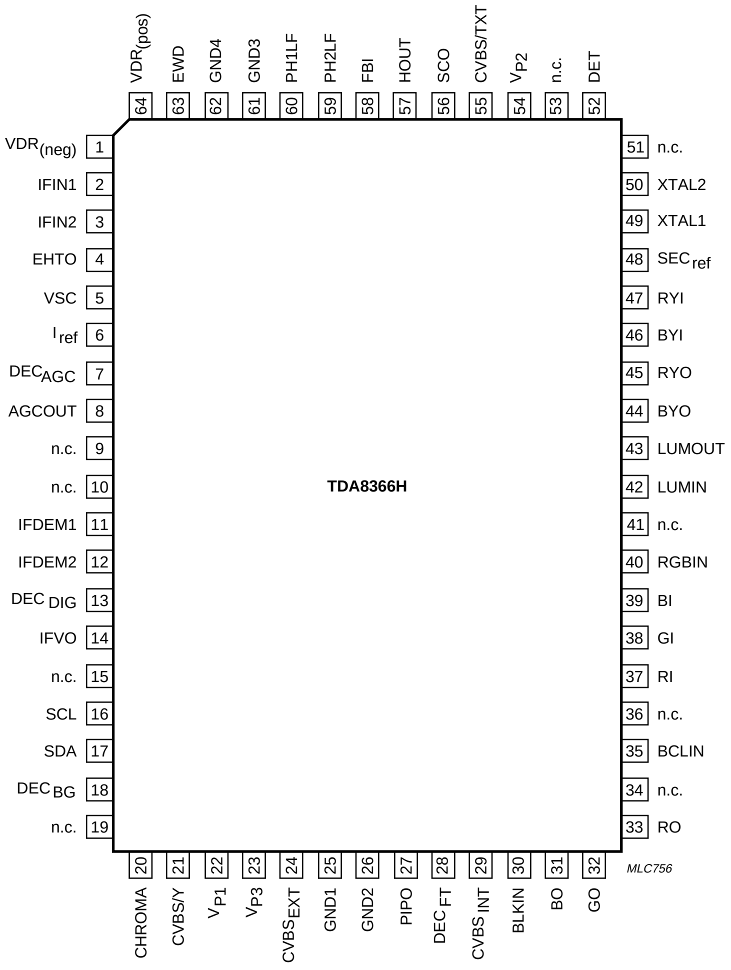



Fig.3 Pin configuration (QFP64).

## FUNCTIONAL DESCRIPTION

### Vision IF amplifier

The IF-amplifier contains 3 AC-coupled control stages with a total gain control range which is in excess of 66 dB. The sensitivity of the circuit is comparable with that of modern IF-ICs. The reference carrier for the video demodulator is obtained by means of passive regeneration of the picture carrier. The external reference tuned circuit is the only remaining adjustment of the IC.

The polarity of the demodulator can be switched via the $I^2C$-bus in such a way that the circuit is suitable for both positive and negative modulated signals.

The AFC-circuit is driven with the same reference signal as the video demodulator. To avoid that the video content disturbs the AFC operation a sample-and-hold circuit is applied for signals with negative modulation. The capacitor for this function is internal. The AFC information is supplied to the tuning system via the $I^2C$-bus.

The AGC-detector operates on top-sync or top white-level depending on the polarity of the demodulator. The demodulation polarity is switched via the $I^2C$-bus. The AGC detector time-constant capacitor is connected externally (this mainly because of the flexibility of the application). The time-constant of the AGC system during positive modulation is rather long to avoid visible variations of the signal amplitude. To obtain an acceptable speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When during 3 frame periods no action is detected the speed of the system is increased.

The circuit contains a video identification circuit which is independent of the synchronization circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor. The identification output is supplied to the tuning system via the $I^2C$-bus. The information of this identification circuit can also be used to switch the phase-1 ($\varphi_1$) loop to a low gain when no signal is received so that a stable OSD display is obtained. The coupling of the video identification circuit with the $\varphi_1$ loop can be switched on and off via the $I^2C$-bus.

### Synchronization circuit

The sync separator is preceded by a controlled amplifier which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage which is operating at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. This coincidence detector is only used to detect whether the line oscillator is synchronized and not for transmitter identification. The first Phase-Locked Loop (PLL) has a very high-statical steepness so that the phase of the picture is independent of the line frequency.

The line oscillator is running at twice the line frequency. The oscillator capacitor is internal. Because of the spreads of internal components an automatic adjustment circuit has been added to the IC. It compares the oscillator frequency with that of the crystal oscillator in the colour decoder.

To protect the horizontal output transistor the horizontal drive is switched-off when a power-on-reset is detected. The frequency of the oscillator is calibrated again when all subaddress bytes have been sent. When the oscillator has the right frequency the calibration stops and the horizontal drive is switched-on again via the soft start procedure (standby bit in normal mode). When the IC is switched-on the same procedure is followed.

When the coincidence detector indicates an out-of-lock situation the calibration procedure is repeated.

The circuit has a second control loop to generate the drive pulses for the horizontal driver stage. During the start-up procedure the duty cycle of the horizontal output pulse increases from 0 to 50% in approximately 100 lines.

The vertical sawtooth generator drives the vertical output and EW correction drive circuits. The geometry processing circuits provide control of horizontal shift, EW width, EW parabola/width ratio, EW corner/parabola ratio, trapezium correction, vertical shift, vertical slope, vertical amplitude, and the S-correction. All these controls can be set via the $I^2C$-bus. The geometry processor has a differential current

output for the vertical drive signal and a single-ended output for the EW drive. Both the vertical drive and the EW drive outputs can be modulated for EHT compensation. The EHT compensation pin is also used for overvoltage protection.

The geometry processor also offers the possibilities for vertical compression (for display of 16 : 9 pictures on a 4 : 3 screen) and vertical expansion (for display of 4 : 3 pictures on a 16 : 9 screen with full picture width, or for display of ‘letter-box’ transmissions on a 4 : 3 screen with full picture height). For the expand mode it is possible to shift the picture vertically (only one fixed position).

Also the de-interlace of the vertical output can be set via the $I^2C$-bus.

To avoid damage of the picture tube when the vertical deflection fails the guard output current of the TDA8350 can be supplied to the sandcastle output. When a failure is detected the RGB-outputs are blanked and a bit is set (NDF) in the status byte of the $I^2C$-bus. When no vertical deflection output stage is connected this guard circuit will also blank the output signals. This can be overruled by means of the EVG bit of subaddress 0A (see Table 1).

**Integrated video filters**

The circuit contains a chrominance bandpass and trap circuit. The chrominance trap filter in the luminance path is designed for a symmetrical step response behaviour. The filters are realized by means of gyrator circuits and they are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. The luminance delay line and the delay for the peaking circuit are also realized by means of gyrator circuits.

It is possible to connect a Colour Transient Improvement (CTI) or Picture Signal Improvement (PSI) IC to the TDA8366. Therefore the luminance signal which has passed the filter and delay line circuit is externally available. The output signal of the transient improvement circuit must be supplied to the luminance input circuit. When the CTI function is not required the two pins must be AC-coupled.

**Video switches**

The circuit has two CVBS inputs and an Super-Video Home System (S-VHS) input. The input can be chosen by the $I^2C$-bus. The input selector also has a position in which $CVBS_{EXT}$ is processed, unless there is a signal on the S-VHS input. When the input selector is in this position it switches to the S-VHS input if the S-VHS detector detects sync pulses on the S-VHS luminance input. The S-VHS detector output can be read by the $I^2C$-bus. When the S-VHS option is not used the luminance input can be used as a second input for external CVBS signals. The choice is made via the CVS-bit (see Table 1).

The video switch circuit has two outputs which can be programmed in a different way. The input signal for the decoder is also available on the TXT output. Therefore this signal can be used to drive the teletext decoder and the SECAM add-on decoder. The signal on the PIP output can be chosen independent of the TXT output. If S-VHS is selected for one of the outputs the luminance and chrominance signals are added so that a CVBS signal is obtained again.

**Colour decoder**

The colour decoder contains an alignment-free crystal oscillator, a killer circuit and the colour difference demodulators. The 90° phase shift for the reference signal is made internally. The demodulation angle and gain ratio for the colour difference signals for PAL and NTSC are adapted to the standard.

The colour decoder is very flexible. Together with the SECAM decoder TDA8395 an automatic multistandard decoder can be designed.

Which standard the IC can decode depends on the external crystals. If a 4.4 MHz and a 3.5 MHz crystal are used PAL 4.4, NTSC 4.4, NTSC 3.5 and PAL 3.5 can be decoded. If two 3.5 MHz crystals are used PAL N and M can be decoded. If one crystal is connected only PAL/NTSC 4.4 or PAL/NTSC 3.5 can be decoded. The crystal frequency of the decoder is used to tune the line oscillator. Therefore the value of the crystal frequency must be given to the IC via the $I^2C$-bus.

### RGB output circuit and black-current stabilization

The colour-difference signals are matrixed with the luminance signal to obtain the RGB-signals. For the RGB-inputs linear amplifiers have been chosen so that the circuit is suited for signals coming from the SCART connector. The contrast and brightness control operate on internal and external signals.

The output signal has an amplitude of approximately 2 V black-to-white at nominal input signals and nominal settings of the controls.

The black current stabilization is realized by means of a feedback from the video output amplifiers to the RGB control circuit. The 'black current' of the 3 guns of the picture tube is internally measured and stabilized. The black level control is active during 4 lines at the end of the vertical blanking. During the first line the leakage current is measured and the following 3 lines the 3 guns are adjusted to the required level. The maximum acceptable leakage current is ±100 µA. The nominal value of the 'black current' is 10 µA. The ratio of the currents for the various guns automatically tracks with the white point adjustment so that the back-ground colour is the same as the adjusted white point.

The input impedance of the 'black-current' measuring pin is 15 kΩ. Therefore the beam current during scan will cause the input voltage to exceed the supply voltage. The internal protection will start conducting so that the excessive current is bypassed.

When the TV receiver is switched-on the black current stabilization circuit is not active, the RGB outputs are blanked and beam current limiting input pin is short-circuited. Only during the measuring lines will the outputs supply a voltage of 5 V to the video output stage so that it can be detected if the picture tube is warming up. These pulses are switched-on after a waiting time of approximately 0.5 s. This ensures that the vertical deflection is activated so that the measuring pulses are not visible on the screen. As soon as the current supplied to the measuring input exceeds a value of 190 µA the stabilization circuit is activated. After a waiting time of approximately 0.8 s the blanking and the beam current limiting input pin are released. The remaining switch-on behaviour of the picture is determined by the external time constant of the beam current limiting network.

## I$^2$C-BUS SPECIFICATION

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | X |

MLA743

X = don't care.

Fig.4 Slave address (8A).

Valid subaddresses: 00 to 13; subaddress FE is reserved for test purposes. Auto-increment mode is available for subaddresses.

### Start-up procedure

Read the status bytes until POR = 0 and send all subaddress bytes. The horizontal output signal is switched-on when the oscillator is calibrated. It is possible to have the horizontal output signal available before calibration. Then the SFM bit must be set to logic 0.

Each time before the data in the IC is refreshed, the status bytes must be read. If POR = 1, the procedure mentioned above must be carried out to restart the IC.

When this procedure is not followed the horizontal frequency may be incorrect after power-up or after a power dip.

### Inputs

**Table 1** Input status bits; note 1

| FUNCTION | SUBADDRESS (HEX) | DATA BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Source select | 00 | INA | INB | INC | IND | FOA | FOB | XA | XB |
| Decoder mode | 01 | FORF | FORS | DL | STB | POC | CM2 | CM1 | CM0 |
| Hue | 02 | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| Horizontal shift (HS) | 03 | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| EW width (EW) | 04 | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| EW parabola/width (PW) | 05 | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| EW corner parabola (CP) | 06 | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| EW trapezium (TC) | 07 | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| Vertical slope (VS) | 08 | NCIN | X | A5 | A4 | A3 | A2 | A1 | A0 |
| Vertical amplitude (VA) | 09 | VID | LBM | A5 | A4 | A3 | A2 | A1 | A0 |
| S-correction (SC) | 0A | HCO | EVG | A5 | A4 | A3 | A2 | A1 | A0 |
| Vertical shift (VSH) | 0B | SBL | PRD | A5 | A4 | A3 | A2 | A1 | A0 |
| White point R | 0C | EXP | CL | A5 | A4 | A3 | A2 | A1 | A0 |
| White point G | 0D | SFM | CVS | A5 | A4 | A3 | A2 | A1 | A0 |
| White point B | 0E | MAT | PHL | A5 | A4 | A3 | A2 | A1 | A0 |
| Peaking | 0F | YD3 | YD2 | YD1 | YD0 | A3 | A2 | A1 | A0 |
| Brightness | 10 | RBL | COR | A5 | A4 | A3 | A2 | A1 | A0 |
| Saturation | 11 | IE1 | X | A5 | A4 | A3 | A2 | A1 | A0 |
| Contrast | 12 | AFW | IFS | A5 | A4 | A3 | A2 | A1 | A0 |
| AGC take-over | 13 | MOD | VSW | A5 | A4 | A3 | A2 | A1 | A0 |

**Note**

1. X = don’t care.

**Table 2** Output status bits; note 1

| FUNCTION | SUBADDRESS (HEX) | DATA BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Output status bytes | 00 | POR | FSI | STS | SL | XPR | CD2 | CD1 | CD0 |
| | 01 | NDF | IN1 | X | IFI | AFA | AFB | X | X |

**Note**

1. X = don’t care.

INPUT CONTROL BITS

**Table 3** Source select 1

| INA | INB | DECODER AND TXT |
|---|---|---|
| 0 | 0 | $CVBS_{INT}$ |
| 0 | 1 | $CVBS_{EXT}$ |
| 1 | 0 | S-VHS |
| 1 | 1 | S-VHS ($CVBS_{EXT}$) |

**Table 4** Source select 2

| INC | IND | PIP |
|---|---|---|
| 0 | 0 | $CVBS_{INT}$ |
| 0 | 1 | $CVBS_{EXT}$ |
| 1 | 0 | S-VHS |
| 1 | 1 | S-VHS ($CVBS_{EXT}$) |

**Table 5** Phase 1 ($\varphi_1$) time constant

| FOA | FOB(1) | MODE |
|---|---|---|
| 0 | 0 | normal |
| 0 | 1 | slow |
| 1 | X | fast |

**Note**

1. X = don’t care.

**Table 6** Crystal indication

| XA | XB | CRYSTAL |
|---|---|---|
| 0 | 0 | two 3.6 MHz |
| 0 | 1 | one 3.6 MHz (pin 32) |
| 1 | 0 | one 4.4 MHz (pin 33) |
| 1 | 1 | 3.6 MHz (pin 32) and 4.4 MHz (pin 33) |

**Table 7** Forced field frequency

| FORF | FORS | FIELD FREQUENCY |
|---|---|---|
| 0 | 0 | auto (60 Hz when line not synchronized) |
| 0 | 1 | 60 Hz; note 1 |
| 1 | 0 | 50 Hz; note 1 |
| 1 | 1 | auto (50 Hz when line not synchronized) |

**Note**

1. When the forced mode is selected the divider will only switch to that position when the horizontal oscillator is not synchronized.

**Table 8** Interlace

| DL | STATUS |
|---|---|
| 0 | interlace |
| 1 | de-interlace |

**Table 9** Standby

| STB | MODE |
|---|---|
| 0 | standby |
| 1 | normal |

**Table 10** Synchronization mode

| POC | MODE |
|---|---|
| 0 | active |
| 1 | not active |

**Table 11** Colour decoder mode

| CM2 | CM1 | CM0 | DECODER MODE |
|---|---|---|---|
| 0 | 0 | 0 | not forced, own intelligence |
| 0 | 0 | 1 | forced NTSC 3.6 MHz |
| 0 | 1 | 0 | forced PAL 4.4 MHz |
| 0 | 1 | 1 | forced SECAM |
| 1 | 0 | 0 | forced NTSC 4.4 MHz |
| 1 | 0 | 1 | forced PAL 3.6 MHz (pin 32) |
| 1 | 1 | 0 | forced PAL 3.6 MHz (pin 33) |
| 1 | 1 | 1 | no function |

**Table 12** Vertical divider mode

| NCIN | VERTICAL DIVIDER MODE |
|---|---|
| 0 | normal operation |
| 1 | switched to search window |

**Table 13** Video ident mode

| VID | VIDEO IDENT MODE |
|---|---|
| 0 | $\varphi_1$ loop switched on and off |
| 1 | not active |

**Table 14** Long blanking mode

| LBM | BLANKING MODE |
|---|---|
| 0 | adapted to standard (50 or 60 Hz) |
| 1 | fixed in accordance with 50 Hz standard |

**Table 15** EHT tracking mode

| HCO | TRACKING MODE |
|---|---|
| 0 | EHT tracking only on vertical |
| 1 | EHT tracking on vertical and EW |

**Table 16** Enable vertical guard (RGB blanking)

| EVG | VERTICAL GUARD MODE |
|---|---|
| 0 | not active |
| 1 | active |

**Table 17** Service blanking

| SBL | SERVICE BLANKING MODE |
|---|---|
| 0 | off |
| 1 | on |

**Table 18** Overvoltage input mode

| PRD | OVERVOLTAGE MODE |
|---|---|
| 0 | detection mode |
| 1 | protection mode |

**Table 19** Vertical deflection mode

| EXP | CL | VERTICAL DEFLECTION MODE |
|---|---|---|
| 0 | 0 | normal |
| 0 | 1 | compress |
| 1 | 0 | expand |
| 1 | 1 | expand and lift |

**Table 20** Horizontal frequency during switch-on

| SFM | START-UP FREQUENCY |
|---|---|
| 0 | maximum |
| 1 | nominal |

**Table 21** Condition Y/C input

| CVS | Y-INPUT MODE |
|---|---|
| 0 | switched to Y/C mode |
| 1 | switched to CVBS mode |

**Table 22** PAL/NTSC matrix

| MAT | MATRIX |
|---|---|
| 0 | adapted to standard |
| 1 | PAL |

**Table 23** Colour crystal PLL

| PHL | STATE |
|---|---|
| 0 | PLL closed |
| 1 | oscillator free-running |

**Table 24** Y-delay adjustment; note 1

| YD0 to YD3 | Y-DELAY |
|---|---|
| YD3 | YD3 ∗ 160 ns + |
| YD2 | YD2 ∗ 80 ns + |
| YD1 | YD1 ∗ 40 ns + |
| YD0 | YD0 ∗ 40 ns |

**Note**

1. For an equal delay of the luminance and chrominance signal the delay must be set at a value of 160 ns. This is only valid for a CVBS signal without group delay distortions.

**Table 25** RGB blanking

| RBL | RGB BLANKING |
|---|---|
| 0 | not active |
| 1 | active |

**Table 26** Noise coring (peaking)

| COR | NOISE CORING |
|---|---|
| 0 | off |
| 1 | on |

**Table 27** Enable fast blanking

| IE1 | FAST BLANKING |
|---|---|
| 0 | not active |
| 1 | active |

**Table 28** AFC window

| AFW | AFC WINDOW |
|---|---|
| 0 | normal |
| 1 | enlarged |

**Table 29** IF sensitivity

| IFS | IF SENSITIVITY |
|---|---|
| 0 | normal |
| 1 | reduced |

**Table 30** Modulation standard

| MOD | MODULATION |
|---|---|
| 0 | negative |
| 1 | positive |

**Table 31** Video mute

| VSW | STATE |
|---|---|
| 0 | normal operation |
| 1 | IF-video signal switched off |

OUTPUT CONTROL BITS

**Table 32** Power-on-reset

| POR | MODE |
|---|---|
| 0 | normal |
| 1 | power-down |

**Table 33** Field frequency indication

| FSI | FREQUENCY |
|---|---|
| 0 | 50 Hz |
| 1 | 60 Hz |

**Table 34** S-VHS status

| STS | S-VHS INPUT |
|---|---|
| 0 | no signal |
| 1 | signal |

**Table 35** Phase 1 ($\varphi_1$) lock indication

| SL | INDICATION |
|---|---|
| 0 | not locked |
| 1 | locked |

**Table 36** X-ray protection

| XPR | OVERVOLTAGE |
|---|---|
| 0 | no overvoltage detected |
| 1 | overvoltage detected |

**Table 37** Colour decoder mode

| CD2 | CD1 | CD0 | STANDARD |
|---|---|---|---|
| 0 | 0 | 0 | no colour standard identified |
| 0 | 0 | 1 | NTSC 3.6 MHz |
| 0 | 1 | 0 | PAL 4.4 MHz |
| 0 | 1 | 1 | SECAM |
| 1 | 0 | 0 | NTSC 4.4 MHz |
| 1 | 0 | 1 | PAL 3.6 MHz (pin 32) |
| 1 | 1 | 0 | PAL 3.6 MHz (pin 33) |
| 1 | 1 | 1 | spare |

**Table 38** Output vertical guard

| NDF | VERTICAL OUTPUT STAGE |
|---|---|
| 0 | OK |
| 1 | failure |

**Table 39** Indication RGB insertion

| IN1 | RGB INSERTION |
|---|---|
| 0 | no (pin 24 LOW) |
| 1 | yes (pin 24 HIGH) |

**Table 40** Output video identification

| IFI | VIDEO SIGNAL |
|---|---|
| 0 | no video signal identified |
| 1 | video signal identified |

**Table 41** AFC output

| AFA | AFB | CONDITION |
|---|---|---|
| 0 | 0 | outside window; too low |
| 0 | 1 | outside window; too high |
| 1 | 0 | in window; below reference |
| 1 | 1 | in window; above reference |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_P$ | supply voltage | | – | 9.0 | V |
| $T_{stg}$ | storage temperature | | –25 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | 0 | 70 | °C |
| $T_{sol}$ | soldering temperature | for 5 s | – | 260 | °C |
| $T_j$ | operating junction temperature | | – | 150 | °C |
| $V_{es}$ | electrostatic handling | HBM; all pins; notes 1 and 2 | –2000 | +2000 | V |
| | | MM; all pins; notes 1 and 3 | –200 | +200 | V |

**Notes**

1. All pins are protected against ESD by means of internal clamping diodes.
2. Human Body Model (HBM): R = 1.5 kΩ; C = 100 pF.
3. Machine Model (MM): R = 0 Ω; C = 200 pF.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th\ j\text{-}a}$ | thermal resistance from junction to ambient in free air | | |
| | SDIP52 | 40 | K/W |
| | QFP64 | 50 | K/W |

## QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611E”*. The number of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9398 510 63011.

### Latch-up

- $I_{trigger}$ ≥ 100 mA or ≥1.5$V_{DD(max)}$
- $I_{trigger}$ ≤ –100 mA or ≤–0.5$V_{DD(max)}$.

Following pins do not meet the above specification:

Pin 7: –90 mA
Pin 17: 90 mA
Pin 18: 90 mA
Pin 19: 90 mA
Pin 24: –90 mA
Pin 34: 60 mA
Pin 49: –90 mA
Pin 50: ±90 mA.

## CHARACTERISTICS

$V_P$ = 8 V; $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| MAIN SUPPLY (PIN 10) | | | | | | |
| $V_{P1}$ | supply voltage | | 7.2 | 8.0 | 8.8 | V |
| $I_{P1}$ | supply current | | – | 100 | – | mA |
| $P_{tot}$ | total power dissipation | | – | 850 | – | W |
| HORIZONTAL OSCILLATOR SUPPLY (PIN 35) | | | | | | |
| $V_{P2}$ | supply voltage | | 7.2 | 8.0 | 8.8 | V |
| $I_{P2}$ | supply current | | – | 6 | – | mA |
| **IF circuit** | | | | | | |
| VISION IF AMPLIFIER INPUTS (PINS 46 AND 47) | | | | | | |
| $V_{i(rms)}$ | input sensitivity (RMS value) | note 1 | | | | |
| | | $f_i$ = 38.90 MHz | – | 70 | 100 | μV |
| | | $f_i$ = 45.75 MHz | – | 70 | 100 | μV |
| | | $f_i$ = 58.75 MHz | – | 70 | 100 | μV |
| $R_I$ | input resistance (differential) | note 2 | – | 2 | – | kΩ |
| $C_I$ | input capacitance (differential) | note 2 | – | 3 | – | pF |
| $G_{cr}$ | gain control range | | 64 | – | – | dB |
| $V_{i\,max(rms)}$ | maximum input signal (RMS value) | | 100 | 150 | – | mV |
| VIDEO AMPLIFIER OUTPUT (PIN 4); note 3 | | | | | | |
| $V_o$ | zero signal output level | negative modulation; note 4 | – | 4.7 | – | V |
| | | positive modulation; note 4 | – | 2.0 | – | V |
| $V_4$ | top sync level | negative modulation | 1.9 | 2.0 | 2.1 | V |
| $V_4$ | white level | positive modulation | – | 4.5 | – | V |
| $\Delta V_4$ | difference in amplitude between negative and positive modulation | | – | 0 | 15 | % |
| $Z_o$ | video output impedance | | – | 50 | – | Ω |
| $I_{bias}$ | internal bias current of NPN emitter follower output transistor | | 1.0 | – | – | mA |
| $I_{source(max)}$ | maximum source current | | – | – | 5 | mA |
| B | bandwidth of demodulated output signal | at –3 dB | 6 | 9 | – | MHz |
| $G_{diff}$ | differential gain | note 5 | – | 2 | 5 | % |
| $\varphi_{diff}$ | differential phase | notes 5 and 6 | – | – | 5 | deg |
| $NL_{vid}$ | video non-linearity | note 7 | – | – | 5 | % |
| $V_{th}$ | white spot threshold level | | – | 5.0 | – | V |
| $V_{ins}$ | white spot insertion level | | – | 3.3 | – | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| VIDEO AMPLIFIER OUTPUT (CONTINUED) | | | | | | |
| $N_{clamp}$ | noise inverter clamping level | | – | 1.4 | – | V |
| $N_{ins}$ | noise inverter insertion level (identical to black level) | | – | 2.6 | – | V |
| $\delta_{mod}$ | intermodulation | notes 6 and 8 | | | | |
| | blue | $V_o$ = 0.92 or 1.1 MHz | 60 | 66 | – | dB |
| | | $V_o$ = 2.66 or 3.3 MHz | 60 | 66 | – | dB |
| | yellow | $V_o$ = 0.92 or 1.1 MHz | 56 | 62 | – | dB |
| | | $V_o$ = 2.66 or 3.3 MHz | 60 | 66 | – | dB |
| S/N | signal-to-noise ratio | notes 6 and 9 | | | | |
| | | $V_i$ = 10 mV | 52 | 60 | – | dB |
| | | end of control range | 52 | 61 | – | dB |
| $V_4$ | residual carrier signal | note 6 | – | 5.5 | – | mV |
| $V_4$ | residual 2nd harmonic of carrier signal | note 6 | – | 2.5 | – | mV |
| IF AND TUNER AGC; note 10 | | | | | | |
| *timing of IF-AGC with a 2.2 μF capacitor (pin 51)* | | | | | | |
| | modulated video interference | 30% AM for 1 mV to 100 mV; 0 to 200 Hz (system B/G) | – | – | 10 | % |
| $t_{inc}$ | response time to an IF input signal amplitude increase of 52 dB | positive and negative modulation | – | 2 | – | ms |
| $t_{dec}$ | response to an IF input signal amplitude decrease of 52 dB | negative modulation | – | 50 | – | ms |
| | | positive modulation | – | 100 | – | ms |
| $I_L$ | allowed leakage current of the AGC capacitor | negative modulation | – | – | 10 | μA |
| | | positive modulation | – | – | 200 | nA |
| *Tuner take-over adjustment (via I²C-bus)* | | | | | | |
| $V_{51min(rms)}$ | minimum starting level for tuner take-over (RMS value) | | – | 0.4 | 0.8 | mV |
| $V_{51max(rms)}$ | maximum starting level for tuner take-over (RMS value) | | 40 | 80 | – | mV |
| *Tuner control output (pin 52)* | | | | | | |
| $V_{52max}$ | maximum tuner AGC output voltage | maximum tuner gain; note 2 | – | – | $V_P$ + 1 | V |
| $V_{52(sat)}$ | output saturation voltage | minimum tuner gain; $I_{47}$ = 2 mA | – | – | 300 | mV |
| $I_{52max}$ | maximum tuner AGC output swing | | 5 | – | – | mA |
| $I_L$ | leakage current RF AGC | | – | – | 1 | μA |
| $\Delta V_i$ | input signal variation for complete tuner control | | 0.5 | 2 | 4 | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| AFC OUTPUT (VIA I²C-BUS); note 11 | | | | | | |
| RES | AFC resolution | | – | 2 | – | bits |
| $W_{sen}$ | window sensitivity | | 65 | 80 | 100 | kHz |
| $W_{senL}$ | window sensitivity in large window mode | | 195 | 240 | 300 | kHz |
| $f_{os}$ | AFC offset | note 6 | – | – | 50 | kHz |
| VIDEO IDENTIFICATION OUTPUT (VIA I²C-BUS) | | | | | | |
| $t_d$ | delay time of identification after the AGC has stabilized on a new transmitter | | – | – | 10 | ms |
| **CVBS and S-VHS input switch** | | | | | | |
| INTERNAL AND EXTERNAL CVBS INPUTS (PINS 11 AND 15) | | | | | | |
| $V_{11(p-p)}$ | CVBS input voltage (peak-to-peak value) | note 12 | – | 1.0 | 1.4 | V |
| $I_{11}$ | CVBS input current | | – | 4 | – | µA |
| $SS_{CVBS}$ | suppression of non-selected CVBS input signal | notes 6 and 13 | 50 | – | – | dB |
| S-VHS INPUT (PINS 8 AND 9) | | | | | | |
| $V_{9(p-p)}$ | luminance input voltage (peak-to-peak value) | | – | 1.0 | 1.4 | V |
| $I_{9(p-p)}$ | luminance input current | | – | 4 | – | µA |
| $V_8$ | chrominance input voltage (burst amplitude) | note 14 | – | 0.3 | 0.45 | V |
| $I_8$ | chrominance input current | | – | 4 | – | µA |
| TXT AND PIP OUTPUT SIGNALS (PINS 36 AND 13) | | | | | | |
| $V_{o(p-p)}$ | output signal amplitude (peak-to-peak value) | | – | 1.0 | – | V |
| $Z_o$ | output impedance | | – | – | 250 | Ω |
| $V_{TS}$ | top sync level | | – | 2.5 | – | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **RGB inputs, colour difference inputs, luminance inputs and outputs** | | | | | | |
| RGB INPUTS (PINS 21, 22 AND 23) | | | | | | |
| $V_{21,22,23(p-p)}$ | input signal amplitude for an output signal of 2 V (black-to-white) (peak-to-peak value) | note 15 | – | 0.7 | 0.8 | V |
| $V_{21,22,23(p-p)}$ | input signal amplitude before clipping occurs (peak-to-peak value) | note 6 | 1.0 | – | – | V |
| $\Delta V_o$ | difference between black level of internal and external signals at the outputs | | – | – | 20 | mV |
| $I_{21,22,23}$ | input currents | no clamping; note 2 | – | – | 0.5 | μA |
| $\Delta t_d$ | delay difference for the three channels | note 6 | – | 0 | 20 | ns |
| FAST BLANKING (PIN 24) | | | | | | |
| $V_i$ | input voltage | no data insertion | – | – | 0.4 | V |
| | | data insertion | 0.9 | – | – | V |
| $V_{24(max)}$ | maximum input pulse | insertion | – | – | 3.0 | V |
| $t_d$ | delay time from RGB in to RGB out | data insertion; note 6 | – | 100 | – | ns |
| $\Delta t_d$ | delay difference between insertion to RGB out and RGB in to RGB out | data insertion; note 6 | – | 50 | – | ns |
| $I_{24}$ | input current | | – | – | 0.2 | mA |
| $SS_{int}$ | suppression of internal RGB signals | notes 6 and 12; insertion; $f_i$ = 0 to 5 MHz | 55 | – | – | dB |
| $SS_{ext}$ | suppression of external RGB signals | notes 6 and 12; no insertion; $f_i$ = 0 to 5 MHz | 55 | – | – | dB |
| $V_I$ | input voltage to blank the RGB outputs to facilitate 'On Screen Display' signals being applied to the outputs | | 4 | – | – | V |
| COLOUR DIFFERENCE INPUT SIGNALS (PINS 29 AND 30) | | | | | | |
| $V_{30(p-p)}$ | input signal amplitude (R–Y) (peak-to-peak value) | note 2 | – | 1.05 | – | V |
| $V_{29(p-p)}$ | input signal amplitude (B–Y) (peak-to-peak value) | note 2 | – | 1.35 | – | V |
| $I_{29,30}$ | input current for both inputs | note 2 | – | 0.1 | 1.0 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| LUMINANCE INPUTS AND OUTPUTS (PINS 25 AND 26) | | | | | | |
| $V_{26(p-p)}$ | output signal amplitude (peak-to-peak value) | top sync-white | – | 0.45 | 0.63 | V |
| $V_{TS}$ | top sync level | | – | 2.5 | – | V |
| $Z_o$ | output impedance | | – | 250 | – | Ω |
| $V_{25(p-p)}$ | input signal amplitude (peak-to-peak value) | | – | 0.45 | – | V |
| $I_{clamp}$ | clamp current | during burst key pulse | – | 200 | – | μA |
| $I_i$ | input current | no clamp | – | – | 0.5 | μA |
| **Chrominance filters** | | | | | | |
| CHROMINANCE TRAP CIRCUIT | | | | | | |
| $f_{trap}$ | trap frequency | | – | $f_{osc}$ | – | MHz |
| QF | trap quality factor | note 16 | – | 2 | – | |
| SR | colour subcarrier rejection | | 20 | – | – | dB |
| CHROMINANCE BANDPASS CIRCUIT | | | | | | |
| $f_c$ | centre frequency | | – | $f_{osc}$ | – | MHz |
| QBP | bandpass quality factor | | – | 3 | – | |
| **Delay line and peaking circuit** | | | | | | |
| Y DELAY LINE | | | | | | |
| $t_d$ | delay time | note 6 | – | 480 | – | ns |
| $t_{d1}$ | tuning range delay time | 8 steps | –160 | – | +160 | ns |
| B | bandwidth of internal delay line | note 6 | 5 | – | – | MHz |
| PEAKING CONTROL; note 17 | | | | | | |
| $f_{c(p)}$ | peaking centre frequency | | – | 3 | – | MHz |
| $t_W$ | width of preshoot or overshoot | note 2 | – | 160 | – | ns |
| OS | overshoot | positive | – | 20 | – | % |
| | | negative | – | 36 | – | % |
| | peaking control curve | 16 steps | see Fig.5 | | | |
| CORING STAGE | | | | | | |
| S | coring range | | – | 15 | – | IRE |
| $G_W$ | wave gain | $\frac{\text{negative half wave gain}}{\text{positive half wave gain}}$ | – | 1.8 | – | |
| **Horizontal synchronization circuits** | | | | | | |
| SYNC VIDEO INPUT (PINS 9, 11 AND 15) | | | | | | |
| $V_{9,11,15}$ | sync pulse amplitude | note 2 | 50 | 300 | – | mV |
| $SL_{HS}$ | slicing level for horizontal sync | note 18 | – | 50 | – | % |
| $SL_{VS}$ | slicing level for vertical sync | | – | 30 | – | % |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| HORIZONTAL OSCILLATOR | | | | | | |
| $f_{fr}$ | free running frequency | | – | 15625 | – | Hz |
| $\Delta f_{fr}$ | spread on free running frequency | | – | – | ±2 | % |
| $\Delta f/\Delta V_P$ | frequency variation with respect to the supply voltage | $V_P$ = 8.0 V ±10%; note 6 | – | 0.2 | 0.5 | % |
| $\Delta f_{(max)}$ | frequency variation with temperature | $T_{amb}$ = 0 to 70 °C; note 6 | – | – | 80 | Hz |
| $\Delta f_{osc(max)}$ | maximum frequency deviation at the start of the horizontal output | | – | – | 75 | % |
| FIRST CONTROL LOOP (FILTER CONNECTED TO PIN 41); note 19 | | | | | | |
| $f_{HR}$ | holding range PLL | | – | ±0.9 | ±1.2 | kHz |
| $f_{CR}$ | catching range PLL | note 6 | ±0.6 | ±0.9 | – | kHz |
| S/N | signal-to-noise ratio of the video input signal at which the time constant is switched | | – | 20 | – | dB |
| HYS | hysteresis at the switching point | | – | 1 | – | dB |
| SECOND CONTROL LOOP (CAPACITOR CONNECTED TO PIN 40) | | | | | | |
| $\Delta\varphi_i/\Delta\varphi_o$ | control sensitivity | | – | 150 | – | µs/µs |
| $t_{cr}$ | control range from start of horizontal output to flyback at nominal shift position | | 11 | 12 | – | µs |
| $t_{shift}$ | horizontal shift range | 63 steps | ±2 | – | – | µs |
| | control sensitivity for dynamic compensation | | – | 5.3 | – | µs/V |
| HORIZONTAL OUTPUT (PIN 38); note 20 | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_O$ = 10 mA | – | – | 0.3 | V |
| $I_{O(max)}$ | maximum allowed output current | | 10 | – | – | mA |
| $V_{O(max)}$ | maximum allowed output voltage | | – | – | $V_P$ | V |
| $\delta$ | duty factor | note 6 | – | 50 | – | % |
| FLYBACK PULSE INPUT (PIN 39) | | | | | | |
| $V_{HSW}$ | switching level for horizontal blanking | | – | 0.4 | – | V |
| $V_{\varphi 2(SW)}$ | switching level for phase-2 loop | | – | 4.0 | – | V |
| $V_{39(max)}$ | maximum input voltage | note 2 | – | 8.0 | – | V |
| $Z_i$ | input impedance | note 2 | – | 10 | – | MΩ |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| SANDCASTLE PULSE OUTPUT (PIN 37) | | | | | | |
| $V_{37}$ | output voltage | during burst key | 4.8 | 5.3 | 5.8 | V |
| | | during blanking | 1.8 | 2.0 | 2.2 | V |
| $t_W$ | pulse width | burst key pulse | 3.3 | 3.5 | 3.7 | µs |
| | | vertical blanking (50 Hz) | – | 25 | – | lines |
| | | vertical blanking (60 Hz) | – | 21 | – | lines |
| $V_{clamp}$ | clamp level for vertical guard detection | | – | 2.7 | – | V |
| $I_{37(min)}$ | minimum input current to activate guard detection | | – | – | 0.5 | mA |
| $I_{37(max)}$ | maximum allowable input current | | 2.5 | – | – | mA |
| $t_d$ | delay of start of burst key to start of sync | | – | 5.4 | – | µs |
| SOFT START; note 21 | | | | | | |
| $\delta_{df}$ | duty factor control range | | 0 | – | 50 | % |
| $t_{ss}$ | soft start time | | – | 100 | – | lines |
| **Vertical synchronization and geometry correction** | | | | | | |
| VERTICAL OSCILLATOR; note 22 | | | | | | |
| $f_{fr}$ | free running frequency | | – | 50/60 | – | Hz |
| $f_{lock}$ | locking range | | 45 | – | 64.5 | Hz |
| | divider value not locked | | – | 625/525 | – | lines |
| | locking range | | 488 | – | 722 | lines/ frame |
| VERTICAL RAMP GENERATOR (PIN 49) | | | | | | |
| $V_{49(p-p)}$ | sawtooth amplitude (peak-to-peak value) | VS = 1FH; C = 100 nF; R = 39 kΩ | – | 3.5 | – | V |
| $I_{dis}$ | discharge current | | – | 1 | – | mA |
| $I_{charge}$ | charge current set by external resistor | note 23 | – | 19 | – | µA |
| VS | vertical slope | control range (63 steps) | –14 | – | +14 | % |
| | | compress mode | – | 75 | – | % |
| | | expand mode | – | 133 | – | % |
| $\Delta I_{49}$ | charge current increase | f = 60 Hz | – | 20 | – | % |
| $V_{49L}$ | LOW level of ramp | normal or expand mode | – | 2.07 | – | V |
| | | compress mode | – | 2.55 | – | V |
| VERTICAL DRIVE OUTPUTS (PINS 44 AND 45) | | | | | | |
| $I_{diff(p-p)}$ | differential output current (peak-to-peak value) | VA = 1FH | – | 1 | – | mA |
| $I_{CM}$ | common mode current | | – | 400 | – | µA |
| $V_o$ | output voltage range | | 0 | – | 4.0 | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| EHT TRACKING/OVERVOLTAGE PROTECTION (PIN 48) | | | | | | |
| $\Delta V_{48}$ | input voltage | | 1.2 | – | 2.8 | V |
| SMR | scan modulation range | | –6 | – | +6 | % |
| $\varphi_{vert}$ | vertical sensitivity | | – | 7.5 | – | %/V |
| $\varphi_{EW}$ | EW sensitivity | when switched-on | – | –7.5 | – | %/V |
| $I_{eq}$ | EW equivalent output current | | +120 | – | –120 | μA |
| $V_{48}$ | overvoltage detection level | | – | 3.9 | – | V |
| DE-INTERLACE | | | | | | |
| | first field delay | | – | 0.5H | – | |
| EW WIDTH | | | | | | |
| CR | control range | 63 steps | 100 | – | 80 | % |
| $I_{eq}$ | equivalent output current | | 0 | – | 400 | μA |
| $V_o$ | EW output voltage range | | 1.0 | – | 8.0 | V |
| $I_o$ | EW output current range | | 0 | – | 900 | μA |
| EW PARABOLA/WIDTH | | | | | | |
| CR | control range | 63 steps | 0 | – | 24 | % |
| $I_{eq}$ | equivalent output current | EW = 3FH | 0 | – | 480 | μA |
| EW CORNER/PARABOLA | | | | | | |
| CR | control range | 63 steps | –44 | – | 0 | % |
| $I_{eq}$ | equivalent output current | PW = 3FH; EW = 3FH | –210 | – | 0 | μA |
| EW TRAPEZIUM | | | | | | |
| CR | control range | 63 steps | –4 | – | +4 | % |
| $I_{eq}$ | equivalent output current | | –80 | – | +80 | μA |
| VERTICAL AMPLITUDE | | | | | | |
| CR | control range | 63 steps; SC = 00H | 80 | – | 120 | % |
| | | 63 steps; SC = 3FH | 86 | – | 112 | % |
| $I_{eqdiff(p-p)}$ | equivalent differential vertical drive output current (peak-to-peak value) | SC = 00H | 800 | – | 1200 | μA |
| VERTICAL SHIFT | | | | | | |
| CR | control range | 63 steps | –4 | – | +4 | % |
| $I_{eqdiff(p-p)}$ | equivalent differential vertical drive output current (peak-to-peak value) | | –40 | – | +40 | μA |
| S-CORRECTION | | | | | | |
| CR | control range | 63 steps | 0 | – | 25 | % |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Colour demodulation part** | | | | | | |
| CHROMINANCE AMPLIFIER | | | | | | |
| $ACC_{cr}$ | ACC control range | note 24 | 26 | – | – | dB |
| ΔV | change in amplitude of the output signals over the ACC range | | – | – | 2 | dB |
| $THR_{on}$ | threshold colour killer ON | | –23 | –26 | –29 | dB |
| $HYS_{off}$ | hysteresis colour killer OFF | strong signal conditions; S/N ≥ 40 dB; note 6 | – | +3 | – | dB |
| | | noisy input signals; note 6 | – | +1 | – | dB |
| ACL CIRCUIT | | | | | | |
| | chrominance burst ratio at which the ACL starts to operate | | 2.3 | – | 2.7 | |
| REFERENCE PART | | | | | | |
| *Phase-locked loop;* note 25 | | | | | | |
| $f_{CR}$ | catching range | | 300 | 500 | – | Hz |
| Δφ | phase shift for a ±400 Hz deviation of the oscillator frequency | note 6 | – | – | 2 | deg |
| *Oscillator* | | | | | | |
| $TC_{osc}$ | temperature coefficient of the oscillator frequency | note 6 | – | 2.0 | 2.5 | Hz/K |
| $\Delta f_{osc}$ | oscillator frequency deviation with respect to the supply | note 6; $V_P$ = 8 V ±10% | – | – | 250 | Hz |
| $R_i$ | input resistance | pin 32; f = 3.58 MHz; note 2 | – | 1.5 | – | kΩ |
| | | pin 33; f = 4.43 MHz; note 2 | – | 1.0 | – | kΩ |
| $C_i$ | input capacitance | pins 32 and 33; note 2 | – | – | 10 | pF |
| HUE CONTROL | | | | | | |
| $HUE_{cr}$ | hue control range | 63 steps; see Fig.6 | ±35 | ±40 | – | deg |
| ΔHUE | hue variation for ±10% $V_P$ | note 6 | – | 0 | – | deg |
| ΔHUE/ΔT | hue variation with temperature | $T_{amb}$ = 0 to 70 °C; note 6 | – | 0 | – | deg |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| DEMODULATORS (PINS 27 AND 28) | | | | | | |
| $V_{28(p-p)}$ | (R–Y) output signal amplitude (peak-to-peak value) | note 26 | – | 0.525 | – | V |
| $V_{27(p-p)}$ | (B–Y) output signal amplitude (peak-to-peak value) | note 26 | – | 0.675 | – | V |
| G | gain between both demodulators G(B–Y) and G(R–Y) | | 1.60 | 1.78 | 1.96 | |
| ΔV | spread of signal amplitude ratio PAL/NTSC | note 6 | –1 | – | +1 | dB |
| $Z_o$ | output impedance (R–Y)/(B–Y) output | note 6 | – | 500 | – | Ω |
| B | bandwidth of demodulators | –3 dB; note 27 | – | 650 | – | kHz |
| $V_{27,28(p-p)}$ | residual carrier output (peak-to-peak value) | $f = f_{osc}$; (R–Y) output | | | 5 | mV |
| | | $f = f_{osc}$; (B–Y) output | – | – | 5 | mV |
| | | $f = 2f_{osc}$; (R–Y) output | | | 5 | mV |
| | | $f = 2f_{osc}$; (B–Y) output | – | – | 5 | mV |
| $V_{28(p-p)}$ | H/2 ripple at (R–Y) output (peak-to-peak value) | | – | – | 25 | mV |
| $\Delta V_o/\Delta T$ | change of output signal amplitude with temperature | note 6 | – | 0.1 | – | %/K |
| $\Delta V_o/\Delta V_P$ | change of output signal amplitude with supply voltage | note 6 | – | – | ±0.1 | dB |
| $\varphi_e$ | phase error in the demodulated signals | | – | – | ±5 | deg |
| COLOUR DIFFERENCE MATRICES IN CONTROL CIRCUIT | | | | | | |
| *PAL or (SECAM mode with TDA8395); (R–Y) and (B–Y) not affected* | | | | | | |
| (G–Y)/(R–Y) | ratio of demodulated signals | | – | –0.51 ±10% | – | |
| (G–Y)/(B–Y) | ratio of demodulated signals | | – | –0.19 ±25% | – | |
| *NTSC mode; the colour-difference matrix results in the following signals (nominal hue setting)* | | | | | | |
| (B–Y) | (B–Y) signal | | (B–Y) | | | |
| (R–Y) | (R–Y) signal | | 1.39(R–Y) – 0.07(B–Y) | | | |
| (G–Y) | (G–Y) signal | | –0.46(R–Y) – 0.15(B–Y) | | | |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| REFERENCE SIGNAL OUTPUT FOR TDA8395 (PIN 31) | | | | | | |
| $f_{ref}$ | reference frequency | | – | 4.43 | – | MHz |
| $V_{31(p-p)}$ | output signal amplitude (peak-to-peak value) | | 0.2 | 0.25 | 0.3 | V |
| $V_o$ | output level | PAL/NTSC identified | – | 1.5 | – | V |
| | | no PAL/NTSC identified; SECAM (by TDA8395) identified | – | 5.0 | – | V |
| $I_{31}$ | required current to stop PAL/NTSC identification circuit during SECAM | | 150 | – | – | μA |
| **Control part** | | | | | | |
| SATURATION CONTROL; note 15 | | | | | | |
| $SAT_{cr}$ | saturation control range | 63 steps; see Fig.7 | 52 | – | – | dB |
| CONTRAST CONTROL; note 15 | | | | | | |
| $CON_{cr}$ | contrast control range | 63 steps | – | 20 | – | dB |
| | tracking between the three channels over a control range of 10 dB | see Fig.8 | – | – | 0.5 | dB |
| BRIGHTNESS CONTROL | | | | | | |
| $BRI_{cr}$ | brightness control range | 63 steps; see Fig.9 | – | ±0.7 | – | V |
| RGB AMPLIFIERS (PINS 17, 18 AND 19) | | | | | | |
| $V_{17,18,19(p-p)}$ | output signal amplitude (peak-to-peak value) | at nominal luminance input signal, nominal contrast and white-point adjustment; note 15 | tbf | 2.0 | tbf | V |
| | | at maximum white point setting | – | 3.0 | – | V |
| $V_{BWmax(p-p)}$ | maximum signal amplitude (black-to-white) | note 28 | – | 2.6 | – | V |
| | | at maximum white point setting | – | 3.6 | – | V |
| $V_{RED(p-p)}$ | output signal amplitude for the ‘red’ channel (peak-to-peak value) | at nominal settings for contrast and saturation control and no luminance signal to the input (R–Y, PAL) | tbf | 2.1 | tbf | V |
| $V_{blank}$ | blanking level at the RGB outputs | | 0.7 | 0.8 | 0.9 | V |
| $I_{bias}$ | internal bias current of NPN emitter follower output transistor | | – | 1.5 | – | mA |
| $I_o$ | available output current | | – | 5 | – | mA |
| $Z_o$ | output impedance | | – | 150 | – | Ω |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| RGB AMPLIFIERS (CONTINUED) | | | | | | |
| $CR_{bl}$ | control range of the black-current stabilization | nominal brightness and white-point adjustment (with respect to the measuring pulse); $V_{blk}$ = 2.5 V | – | – | ±1 | V |
| $V_{bl}$ | black level shift with picture content | note 6 | – | – | 20 | mV |
| $V_o$ | output voltage of the 4-L pulse after switch-on | | – | 4.2 | – | V |
| $\Delta bl/\Delta T$ | variation of black level with temperature | note 6 | – | 1.0 | – | mV/K |
| $\Delta bl$ | relative variation in black level between the three channels during variations of | note 6 | | | | |
| | supply voltage (±10%) | nominal controls | – | – | tbf | mV |
| | saturation (50 dB) | nominal contrast | – | – | tbf | mV |
| | contrast (20 dB) | nominal saturation | – | – | tbf | mV |
| | brightness (±0.5 V) | nominal controls | – | – | tbf | mV |
| | temperature (range 40 °C) | | – | – | tbf | mV |
| S/N | signal-to-noise ratio of the output signals | RGB input; note 29 | 60 | – | – | dB |
| | | CVBS input; note 29 | 50 | – | – | dB |
| $V_{res(p-p)}$ | residual voltage at the RGB outputs (peak-to-peak value) | at $f_{osc}$ | – | – | 15 | mV |
| | | at $2f_{osc}$ plus higher harmonics in RGB outputs | – | – | 15 | mV |
| B | bandwidth of output signals | RGB input; at –3 dB | 8 | – | – | MHz |
| | | CVBS input; at –3 dB; $f_{osc}$ = 3.58 MHz | – | 2.8 | – | MHz |
| | | CVBS input; at –3 dB; $f_{osc}$ = 4.43 MHz | – | 3.5 | – | MHz |
| | | S-VHS input; at –3 dB | 5 | – | – | MHz |
| WHITE-POINT ADJUSTMENT | | | | | | |
| | I²C-bus setting for nominal gain | HEX code | – | 20H | – | |
| $G_{inc(max)}$ | maximum increase of the gain | HEX code 3FH | 40 | 50 | 60 | % |
| $G_{dec(max)}$ | maximum decrease of the gain | HEX code 00H | 40 | 50 | 60 | % |
| BLACK-CURRENT STABILIZATION (PIN 16); note 30 | | | | | | |
| $I_{bias}$ | bias current for the picture tube cathode | | – | 10 | – | μA |
| $I_{leak}$ | acceptable leakage current | | – | 100 | – | μA |
| $I_{scan(max)}$ | maximum current during scan | | – | 0.3 | – | mA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| BEAM CURRENT LIMITING (PIN 20); note 28 | | | | | | |
| $V_{CR}$ | contrast reduction starting voltage | | – | 4 | – | V |
| $V_{diffCR}$ | voltage difference for full contrast reduction | | – | 2 | – | V |
| $V_{BR}$ | brightness reduction starting voltage | | – | 3 | – | V |
| $V_{diffBR}$ | voltage difference for full brightness reduction | | – | 2 | – | V |
| $V_{bias}$ | internal bias voltage | | – | 4.5 | – | V |
| $I_{ch(int)}$ | internal charge current | | – | 40 | – | μA |
| $I_{disch}$ | discharge current due to ‘peak-white limiting’ | | – | 200 | – | μA |

**Notes**

1. On set AGC.
2. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
3. Measured at 10 mV (RMS) top sync input signal.
4. So called projected zero point, i.e. with switched demodulator.
5. Measured in accordance with the test line given in Fig.10. For the differential phase test the peak white setting is reduced to 87%.
   a) The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   b) The phase difference is defined as the difference in degrees between the largest and smallest phase angle.
6. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
7. This figure is valid for the complete video signal amplitude (peak white-to-black), see Fig.11.
8. The test set-up and input conditions are given in Fig.12. The figures are measured with an input signal of 10 mV RMS.
9. Measured with a source impedance of 75 Ω, where:

$$S/N = 20 \log \frac{V_O \text{ (black-to-white)}}{V_{m(rms)} \text{ (B = 5 MHz)}}$$

10. To obtain a good noise immunity of the AGC circuit the AGC detector is gated during the sync pulse. This gating is switched-off during the vertical retrace to avoid disturbances of the signal amplitude due to phase errors of the incoming video signal which are caused by the head-switching of VCRs.

11. The AFC slope is directly related to the Q-factor of the demodulator tuned circuit. The given AFC steepness is obtained with a Q-factor of 60. The AFC off-set is tested with a double sideband input signal and with the reference tuned circuit tuned to minimum AGC voltage (optimum tuning for the demodulator).

    The tuning information is supplied to the tuning system via the I²C-bus. Two bits have been reserved for this function. The first bit indicates whether the tuning is within the given window. The second bit indicates the direction of the tuning. Bit indications:

    a) AFA = 1; tuning inside window.

    b) AFA = 0; tuning outside window.

    c) AFB = 1; tuning too high.

    d) AFB = 0; tuning too low.

    To improve the speed of search tuning systems the AFC window can be increased to about 240 kHz. The width of the window can be set by means of the AFW bit in subaddress 03.

12. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
13. This parameter is measured at nominal settings of the various controls.
14. Indicated is a signal for a colour bar with 75% saturation (chroma : burst ratio = 2.2 : 1).
15. Nominal contrast is specified with the DAC in position 20H. Nominal saturation as maximum −10 dB. In the nominal brightness setting the black level at the outputs is identical to the level of the black-current measuring pulses.
16. The −3 dB bandwidth of the circuit can be calculated by means of the following equation:

    $$f_{-3\ dB} = f_{osc}\left(1 - \frac{1}{2Q}\right)$$

17. Valid for a signal amplitude on the Y-input of 0.7 V black-to-white (100 IRE) with a rise time (10% to 90%) of 70 ns and the video switch in the Y/C mode. During production the peaking function is not tested by measuring the overshoots but by measuring the frequency response of the Y output.
18. The slicing level is independent of sync pulse amplitude. The given percentage is the distance between the slicing level and the black level (back porch).
19. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition and the condition of the I²C-bus. Therefore the circuit contains a noise detector and the time constant is switched to ‘slow’ when too much noise is present in the signal. In the ‘fast’ mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible. Switching between the two modes can be automatically or overruled by the I²C-bus.

    The circuit contains a video identification circuit which is independent of first loop. This identification circuit can be used to close or open the first control loop when a video signal is present or not present on the input. This enables a stable On Screen Display (OSD) when just noise is present at the input. The coupling of the video identification circuit with the first loop can be defeated via the I²C-bus.

    When the horizontal PLL is set to the ‘slow’ mode (via I²C-bus bits FOA and FOB) or during weak signal conditions in the ‘automatic’ mode the phase detector is gated to obtain a good noise immunity. The width of the gating pulse is 5.7 µs.

    The output current of the phase detector in the various conditions are shown in Table 42.

20. During the start-up period of the oscillator the duty factor of the output pulse rises gradually from 0% to 50% (time approximately 100 lines).
21. The start-up frequency depends on the SFM bit in the I²C-bus protocol. When SFM = 0 the frequency starts at a high (non calibrated) value. When SFM = 1 the output signal will only be available after calibration.

22. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 3 modes of operation:

    a) Search mode 'large window'.

    This mode is switched on when the circuit is not synchronized or when a non-standard signal (number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz).

    b) Standard mode 'narrow window'.

    This mode is switched on when more than 15 succeeding vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

    c) Standard TV-norm (divider ratio 525 (60 Hz) or 625 (50 Hz).

    When the system is switched to the narrow window it is checked whether the incoming vertical sync pulses are in accordance with the TV-norm. When 15 standard TV-norm pulses are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.

    When 3 vertical sync pulses are missed the system switches back to the narrow window and when also in this window no sync pulses are found (condition 3 missing pulses) the system switches over to the search window.

    The vertical divider needs some waiting time during channel-switching of the tuner. When a fast reaction of the divider is required during channel-switching the system can be forced to the search window by means of the NCIN bit in subaddress 08.

23. Conditions: frequency is 50 Hz; normal mode; VS = 1F.

24. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and −20 dB.

25. All frequency variations are referenced to 3.58 or 4.43 MHz carrier frequency.
    All oscillator specifications are measured with the Philips crystal series 9922 520.
    If the spurious response of the 4.43 MHz crystal is lower than −1 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ, oscillation at the fundamental frequency is guaranteed.
    The spurious response of the 3.58 MHz crystal must be lower than −1 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.

    The catching and detuning range are measured for nominal crystal parameters. These are:

    a) Load resonance frequency $f_0$ = 4.433619 or 3.579545 MHz; $C_L$ = 20 pF.

    b) Motional capacitance $C_1$ = 20.6 fF (4.43 MHz crystal) or 14.7 fF (3.58 MHz crystal).

    c) Parallel capacitance $C_0$ = 5.5 pF (4.43 MHz crystal) or 4.5 pF (3.58 MHz crystal).

    The actual load capacitance in the application should be $C_L$ = 18 pF to account for parasitic capacitances on and off chip.

    Philips Components has developed a special crystal which is tuned to the correct frequency in an application without series capacitance (code number 9922 520 0038X; see Table 43). This has the advantage that the tuning (catching) range is increased with approximately 50% without negative effects on spurious responses. When the catching range of 300 Hz is considered too low this special crystal is a suitable alternative.

    The free-running frequency of the oscillator can be checked by opening the colour PLL via the $I^2C$-bus. In that condition the colour killer is not active so that the frequency off-set is visible on the screen. When two crystals are connected to the IC the circuit must be forced to one of the crystals during this test to prevent the oscillator switching continuously between the two frequencies.

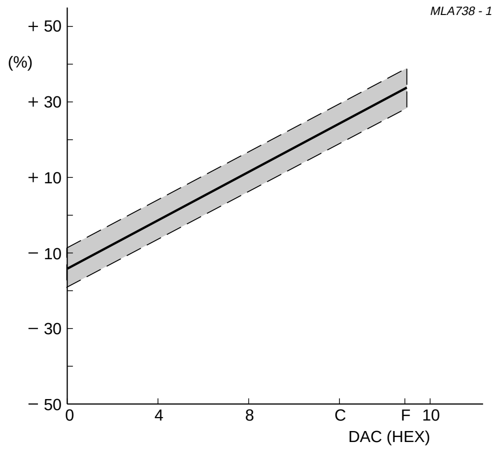
26. The (R–Y) and (B–Y) signals are demodulated with a phase difference of the reference carrier of 90° and a gain ratio $\frac{(B-Y)}{(R-Y)} = 1.78$. The matrixing to the required signals is achieved in the control part.
27. This parameter indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the low-pass filter of the demodulator is approximately 1 MHz.
28. At nominal setting of the gain control. When this amplitude is exceeded the peak-white limiting circuit will reduce the contrast. The control voltage is generated via the external capacitor connected to the beam-current limiting input.
29. Signal-to-noise ratio (S/N) is specified as peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).
30. This is a current input. The indicated value of the nominal bias current is obtained at the nominal setting of the gain (white point) control. The actual value of the bias current depends on the gain control setting of each channel. As a result the 'black-current' of each gun is adapted to the white point setting so that the back-ground colour will follow the white point adjustment.

**Table 42** Output current of the phase detector in the various conditions

| I²C-BUS COMMANDS | | | | IC CONDITIONS | | | φ-1 CURRENT/MODE | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **VID** | **POC** | **FOA** | **FOB** | **IDENT** | **COIN** | **NOISE** | **SCAN** | **V-RETR** | **GATING** | **MODE** |
| – | 0 | 0 | 0 | yes | yes | yes | 30 | 30 | yes | auto |
| – | 0 | 0 | 0 | yes | no | – | 180 | 270 | no | auto |
| – | 0 | 0 | 1 | yes | yes | – | 30 | 30 | yes | slow |
| – | 0 | 0 | 1 | yes | no | – | 180 | 270 | no | slow |
| – | 0 | 1 | – | yes | – | – | 180 | 270 | no | fast |
| 0 | 0 | – | – | no | – | – | 6 | 6 | no | OSD |
| – | 1 | – | – | – | – | – | – | – | – | off |

**Table 43** Code numbers for special crystals

| SYSTEM | FREQUENCY (MHz) | CODE NUMBER |
|---|---|---|
| PAL-N | 3.582056 | 9922 520 00381 |
| NTSC-M | 3.579545 | 9922 520 00382 |
| PAL-M | 3.575611 | 9922 520 00383 |
| PAL-B/G | 4.433619 | 9922 520 00384 |




Overshoot in direction ‘black’.

Fig.5 Peaking control curve.

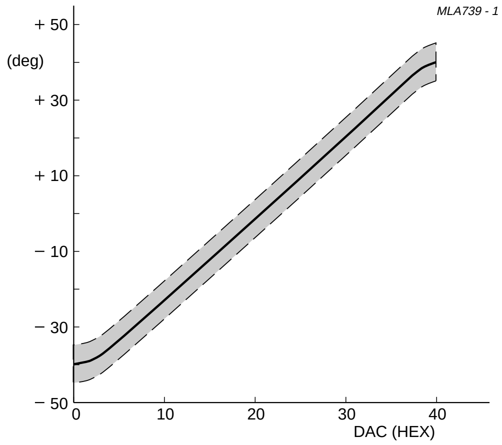



Fig.6 Hue control curve.

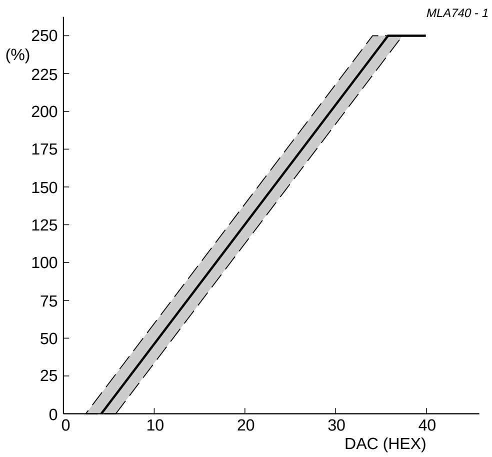



Fig.7 Saturation control curve.

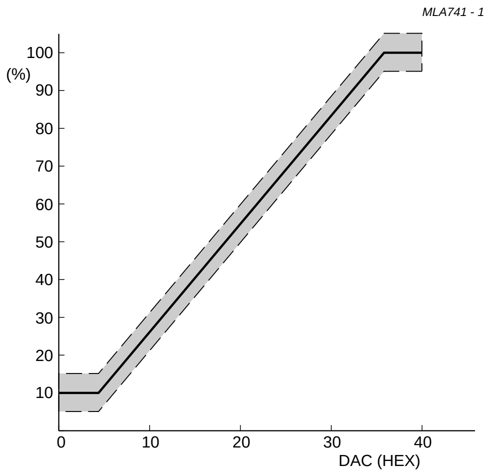
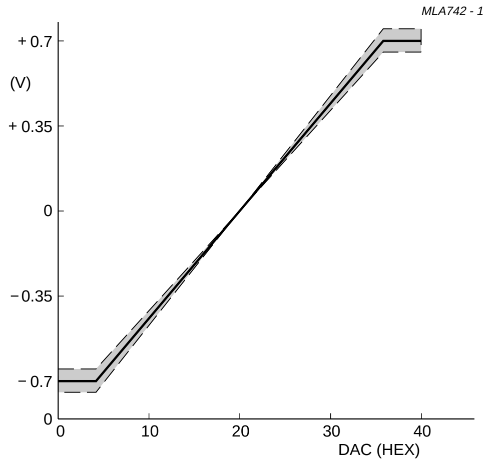



Fig.8 Contrast control curve.




Relative variation with respect to the measuring pulse.

Fig.9 Brightness control curve.

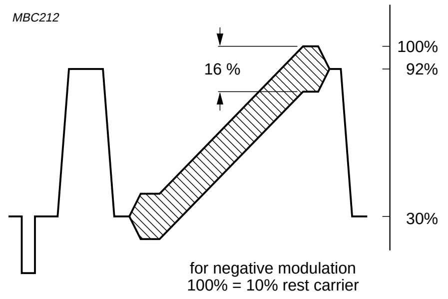



Fig.10 Video output signal.

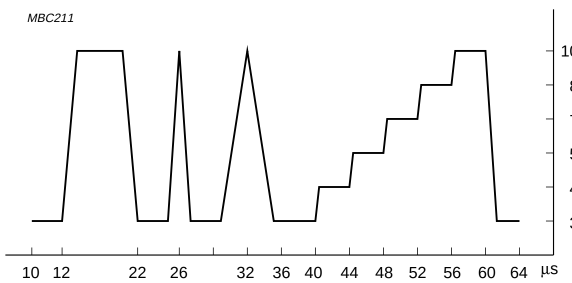
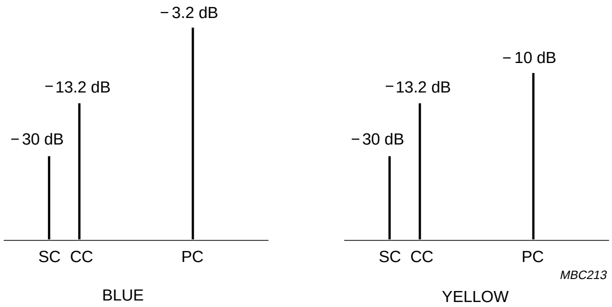
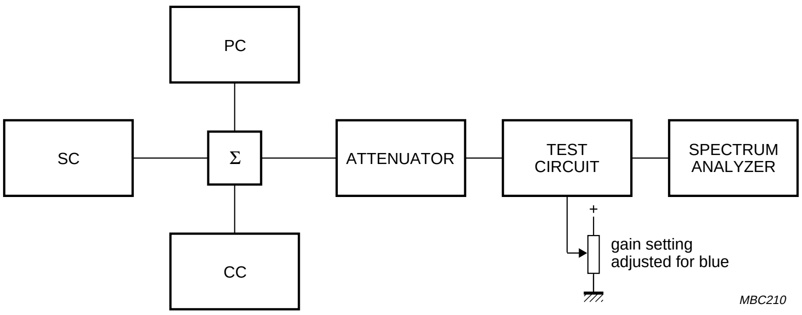



Fig.11 Test signal waveform.




Input signal conditions: SC = sound carrier; CC = colour carrier; PC = picture carrier.
All amplitudes with respect to top sync level.

$$\text{Value at 0.92 or 1.1 MHz} = 20\log\frac{V_O\text{ at 3.58 or 4.4 MHz}}{V_O\text{ at 0.92 or 1.1 MHz}} + 3.6\text{ dB}$$

$$\text{Value at 2.66 or 3.3 MHz} = 20\log\frac{V_O\text{ at 3.58 or 4.4 MHz}}{V_O\text{ at 2.66 or 3.3 MHz}}$$

Fig.12 Test set-up intermodulation.

## TEST AND APPLICATION INFORMATION

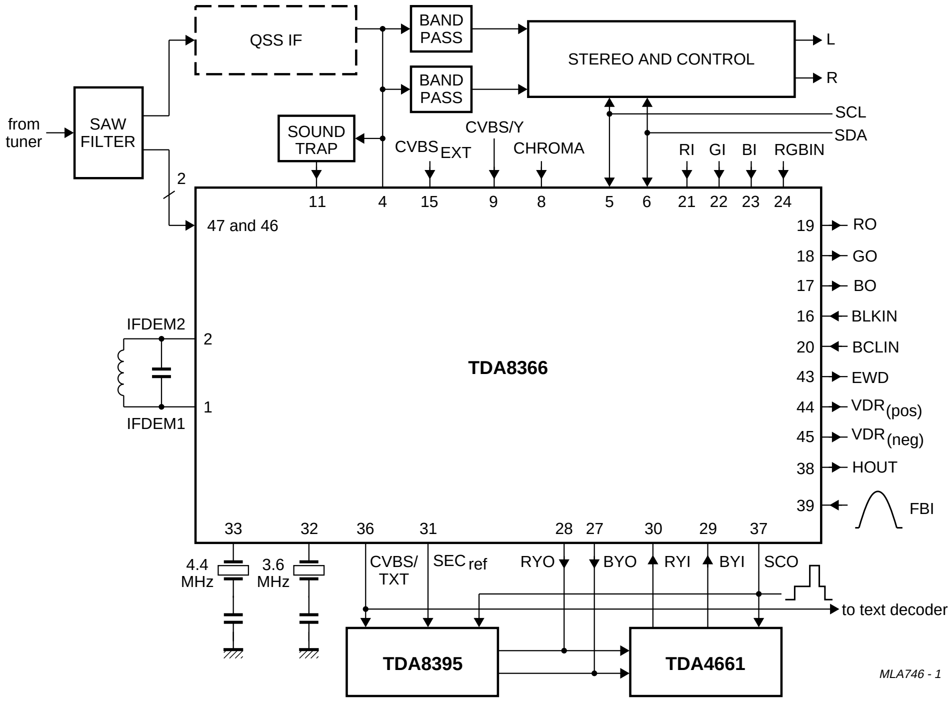



Fig.13 Application diagram.

### East-West output stage

In order to obtain correct tracking of the vertical and horizontal EHT-correction, the EW output stage should be dimensioned as illustrated in Fig.14.

Resistor $R_{EW}$ determines the gain of the EW output stage. Resistor $R_c$ determines the reference current for both the vertical sawtooth generator and the geometry processor.

The preferred value of $R_c$ is 39 kΩ which results in a reference current of 100 μA ($V_{ref}$ = 3.9 V).

The value of $R_{EW}$ must be:

$$R_{EW} = R_c \times \frac{V_{scan}}{18 \times V_{ref}}$$

Example: With $V_{ref}$ = 3.9 V; $R_c$ = 39 kΩ and $V_{scan}$ = 120 V then $R_{EW}$ = 68 kΩ.

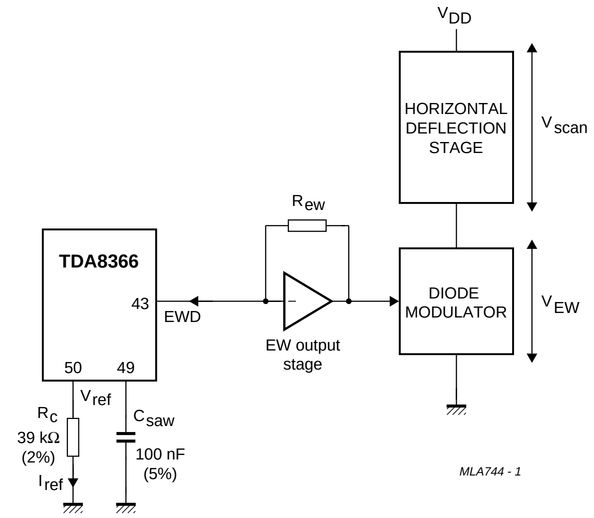
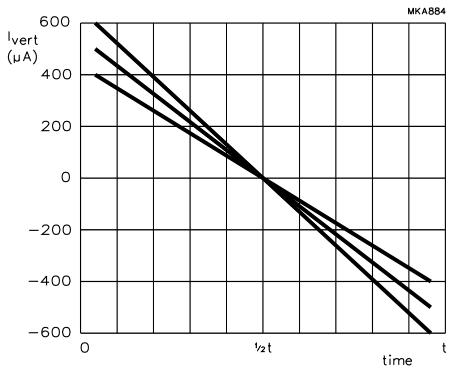
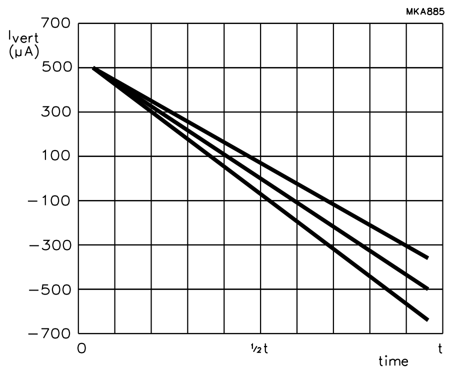



Fig.14 East-West output stage.



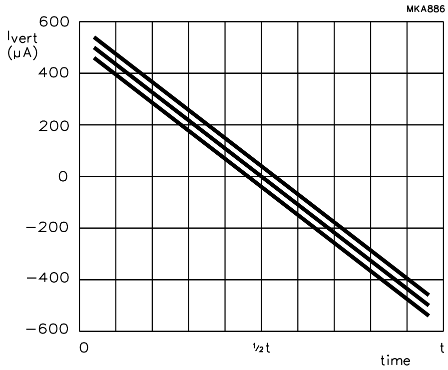

VA = 0, 31H and 63H; VSH = 31H; SC = 0.

Fig.15 Control range of vertical amplitude.



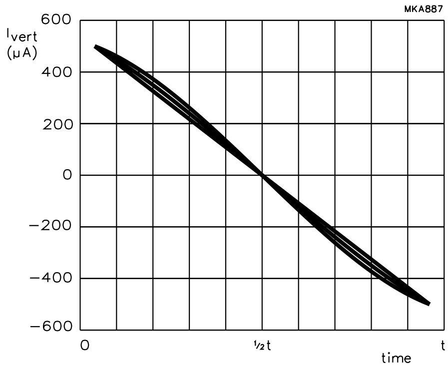

VS = 0, 31H and 63H; VA = 31H; VHS = 31H; SC = 0.

Fig.16 Control range of vertical slope.



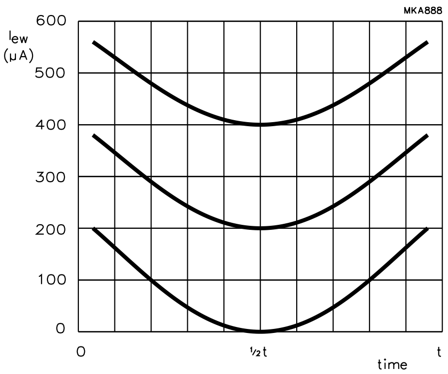

VSH = 0, 31H and 63H; VA = 31H; SC = 0.

Fig.17 Control range of vertical shift.



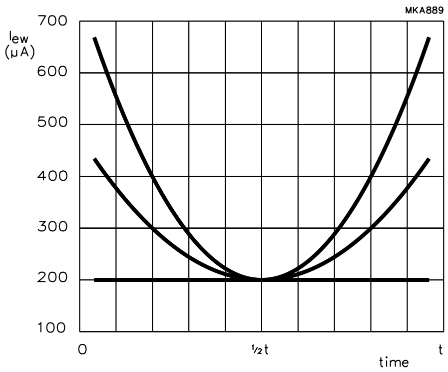

SC = 0, 31H and 63H; VA = 31H; VHS = 31H.

Fig.18 Control range of S-correction.



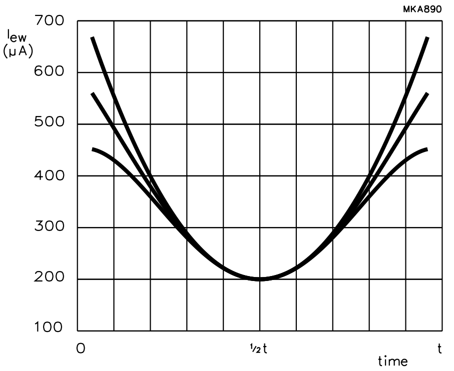

EW = 0, 31H and 63H; PW = 31H; CP = 31H.

Fig.19 Control range of EW width.



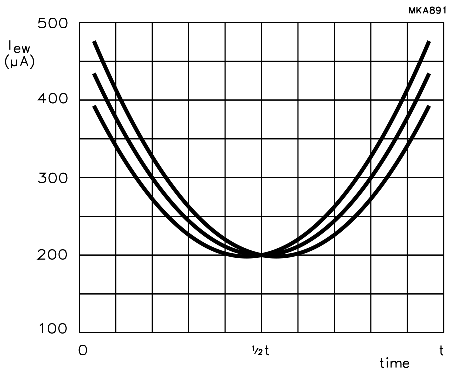

PW = 0, 31H and 63H; EW = 31H; CP = 31H.

Fig.20 Control range of EW parabola/width ratio.




CP = 0, 31H and 63H; EW = 31H; PW = 63H.

Fig.21 Control range of EW corner/parabola ratio.




TC = 0, 31H and 63H; EW = 31H; PW = 31H.

Fig.22 Control range of EW trapezium correction.

**Adjustment of geometry control parameters**

The deflection processor of the TDA8366 offers nine control parameters for picture alignment:

- Vertical picture alignment
  - S-correction
  - vertical amplitude
  - vertical slope
  - vertical shift
- Horizontal picture alignment
  - horizontal shift
  - EW width
  - EW parabola/width
  - EW corner/parabola
  - EW trapezium correction.

It is important to notice that the TDA8366 is designed for use with a DC-coupled vertical deflection stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube type, vertical output stage and EW output stage it is determined which are the required values for the settings of S-correction, EW parabola/width ratio and EW corner/parabola ratio. These parameters can be preset via the $I^2C$-bus, and do not need any additional adjustment. The rest of the parameters are preset with the mid-value of their control range (i.e. 1FH), or with the values obtained by previous TV-set adjustments.

The vertical shift control is meant for compensation of off-sets in the external vertical output stage or in the picture tube. It can be shown that without compensation these off-sets will result in a certain linearity error, especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the value of the off-set, and to the square of the S-correction needed. The necessity to use the vertical shift alignment depends on the expected off-sets in vertical output stage and picture tube, on the required value of the S-correction, and on the demands upon vertical linearity.

For adjustment of the vertical shift and vertical slope independent of each other, a special service blanking mode can be entered by setting the SBL bit HIGH. In this mode the RGB-outputs are blanked during the second half of the picture. There are 2 different methods for alignment of the picture in vertical direction. Both methods make use of the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment the vertical shift should not be changed. The top of the picture is placed by adjustment of the vertical amplitude, and the bottom by adjustment of the vertical slope.

The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). With the vertical slope control the beginning of the blanking is positioned exactly on the middle of the picture. Then the top and bottom of the picture are placed symmetrical with respect to the middle of the screen by adjustment of the vertical amplitude and vertical shift. After this adjustment the vertical shift has the right setting and should not be changed.

If the vertical shift alignment is not required VSH should be set to its mid-value (i.e. VSH = 1F). Then the top of the picture is placed by adjustment of the vertical amplitude and the bottom by adjustment of the vertical slope. After the vertical picture alignment the picture is positioned in the horizontal direction by adjustment of the EW width and the horizontal shift. Finally (if necessary) the left- and right-hand sides of the picture are aligned in parallel by adjusting the EW trapezium control.

After adjustment of the picture for normal vertical deflection as described, no additional adjustment is necessary for the compress and expand mode. If required a small correction of the picture height can be made by adjusting the vertical slope. This will not effect the linearity.